40V N-Ch Power MOSFET

V_{DS}		40	V
$R_{DS(on),typ}$	V_{GS}=10V	1.4	mΩ
$R_{DS(on),typ}$	V_{GS}=4.5V	1.8	mΩ
$I_{D\ (Sillicon\ Limited)}$		181	A
$I_{D\ (Package\ Limited)}$		60	A

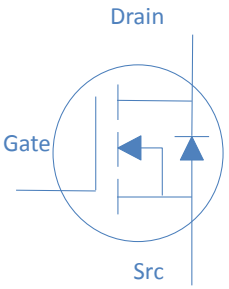
Feature

- Optimized for high speed switching, Logic Level
- Enhanced Body diode dv/dt capability
- Enhanced Avalanche Ruggedness
- 100% UIS Tested, 100% Rg Tested
- Lead Free, Halogen Free

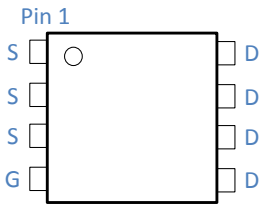
Application

- Synchronous Rectification in SMPS
- Hard Switching and High Speed Circuit
- Power Tools
- UPS
- Motor Control

DFN5x6



Part Number	Package	Marking
HTN020N04P	DFN5x6	TN020N04P



Absolute Maximum Ratings at T_j=25 (unless otherwise specified)

Parameter	Symbol	Conditions	Value	Unit
Continuous Drain Current (Silicon Limited)	I_D	T_C=25	181	A
		T_C=100	115	
Continuous Drain Current (Package Limited)		T_C=25	60	
Drain to Source Voltage	V_{DS}	-	40	V
Gate to Source Voltage	V_{GS}	-	±20	V
Pulsed Drain Current	I_{DM}	-	460	A
Avalanche Energy, Single Pulse	E_{AS}	L=0.4mH, T_C=25	320	mJ
Power Dissipation	P_D	T_C=25	119	W
Operating and Storage Temperature	T_J, T_{stg}	-	-55 to150	

Absolute Maximum Ratings

Parameter	Symbol	Max	Unit
Thermal Resistance Junction-Case	$R_{\theta JC}$	1.05	/W
Thermal Resistance Junction-Ambient	$R_{\theta JA}$	55	/W

Electrical Characteristics at T_j=25 (unless otherwise specified)

Static Characteristics

Parameter	Symbol	Conditions	Value			Unit
			min	typ	max	
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D=250μA	40	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}=V_{DS}, I_D=250μA	1	1.8	2.2	
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS}=0V, V_{DS}=40V, T_j=25	-	-	1	μA
		V_{GS}=0V, V_{DS}=40V, T_j=100	-	-	100	
Gate to Source Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
Drain to Source on Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=20A	-	1.4	2	mΩ
		V_{GS}=4.5V, I_D=20A	-	1.8	3	mΩ
Transconductance	g_{fs}	V_{DS}=5V, I_D=20A	-	120	-	S
Gate Resistance	R_G	V_{GS}=0V, V_{DS} Open, f=1MHz	-	0.85	-	Ω

Dynamic Characteristics

Input Capacitance	C_{iss}	V_{GS}=0V, V_{DS}=20V, f=1MHz	-	7356	-	pF
Output Capacitance	C_{oss}		-	814	-	
Reverse Transfer Capacitance	C_{rss}		-	547	-	
Total Gate Charge (10V)	Q_g (10V)	V_{DD}=20V, I_D=20A, V_{GS}=10V	-	135	-	nC
Total Gate Charge (4.5V)	Q_g (4.5V)		-	70	-	
Gate to Source Charge	Q_{gs}		-	20	-	
Gate to Drain (Miller) Charge	Q_{gd}		-	35	-	
Turn on Delay Time	$t_{d(on)}$	V_{DD}=20V, I_D=20A, V_{GS}=10V, R_G=10Ω,	-	26	-	ns
Rise time	t_r		-	21	-	
Turn off Delay Time	$t_{d(off)}$		-	75	-	
Fall Time	t_f		-	25	-	

Reverse Diode Characteristics

Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_F=20A	-	0.9	1.2	V
Reverse Recovery Time	t_{rr}	V_R=20V, I_F=20A, dI_F/dt=200A/μs	-	40	-	ns
Reverse Recovery Charge	Q_{rr}		-	50	-	nC

Figure 3. On-Resistance vs. Drain Current and Gate Voltage

Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

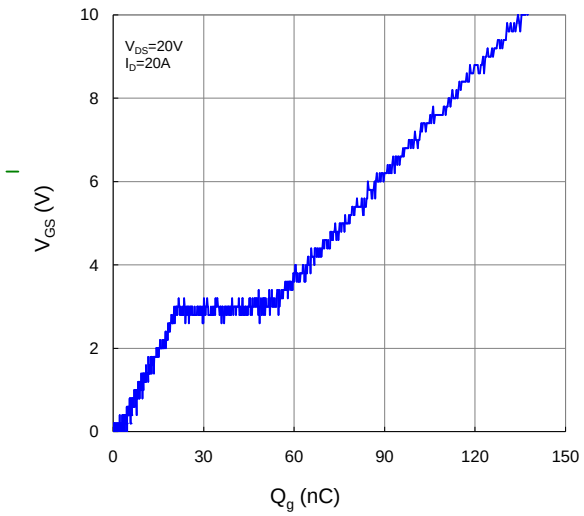


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

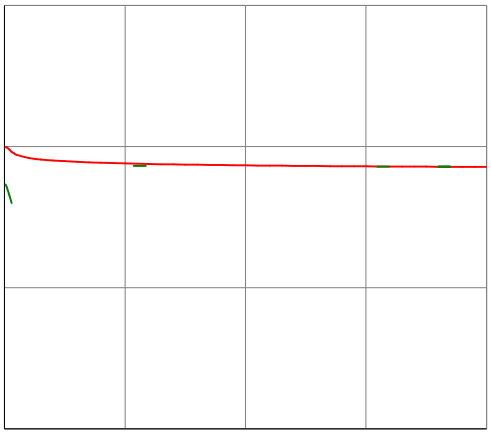
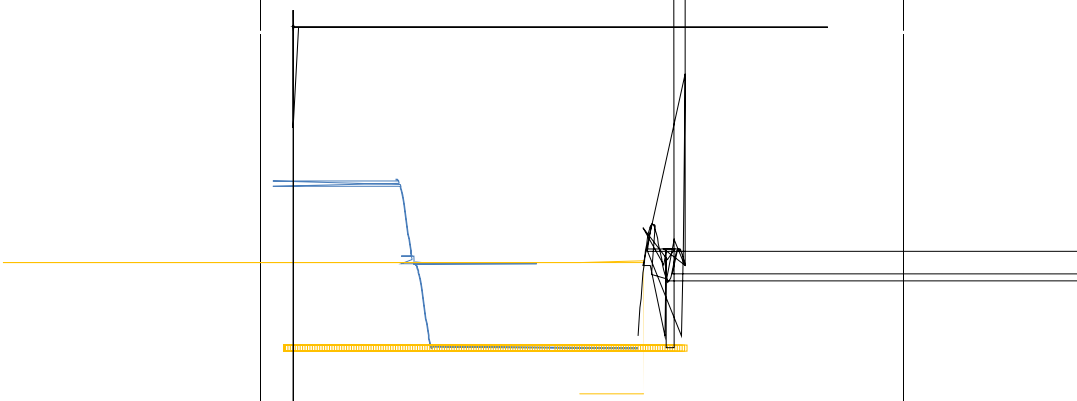


Figure 9. Maximum Safe Operating Area

Figure 10. Maximun Drain Current vs. Case Temperature

Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Case

Inductive switching Test



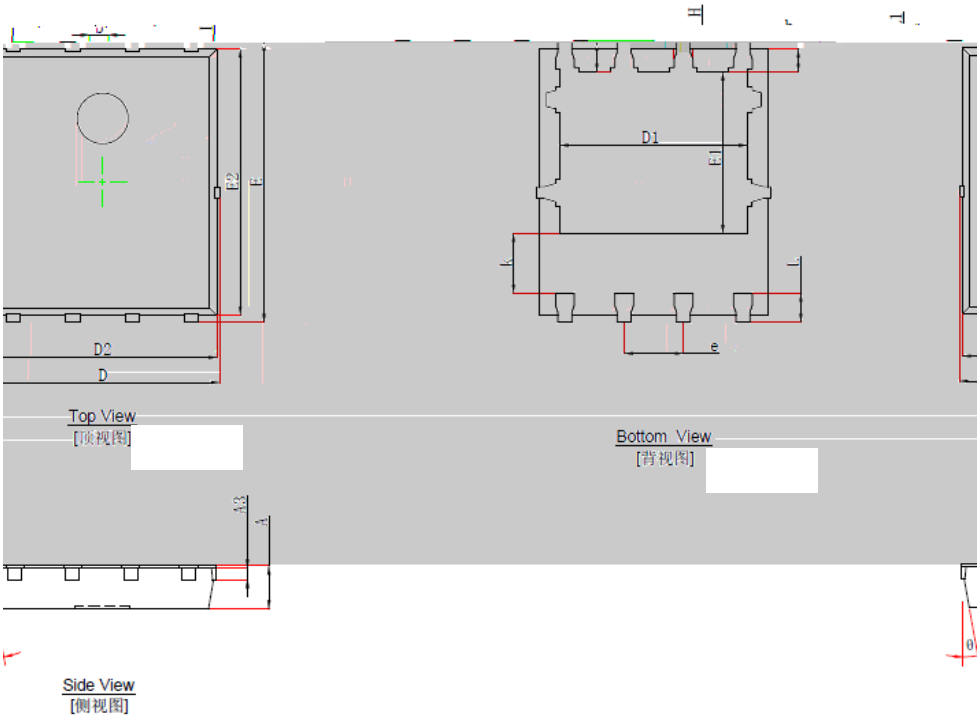
Gate Charge Test

Uclamped Inductive Switching (UIS) Test

Diode Recovery Test

Package Outline

DFN5x6_P, 8 Leads



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039
A3	0.254REF.		0.010REF.	
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	3.910	4.110	0.154	0.162
E1	3.375	3.575	0.133	0.141
D2	4.824	4.976	0.190	0.196
0.229	E2	5.674	5.926	0.223
0.055		1.190	1.390	0.047